



**SUBSTITUTE Drawing Sheet 1 of 10**

**Title:** SELF-ALIGNED TRIPLE GATE SILICON-ON-INSULATOR DEVICE

**Inventors:** Krivokapic et al.

**Appl No.:** 09/711,445

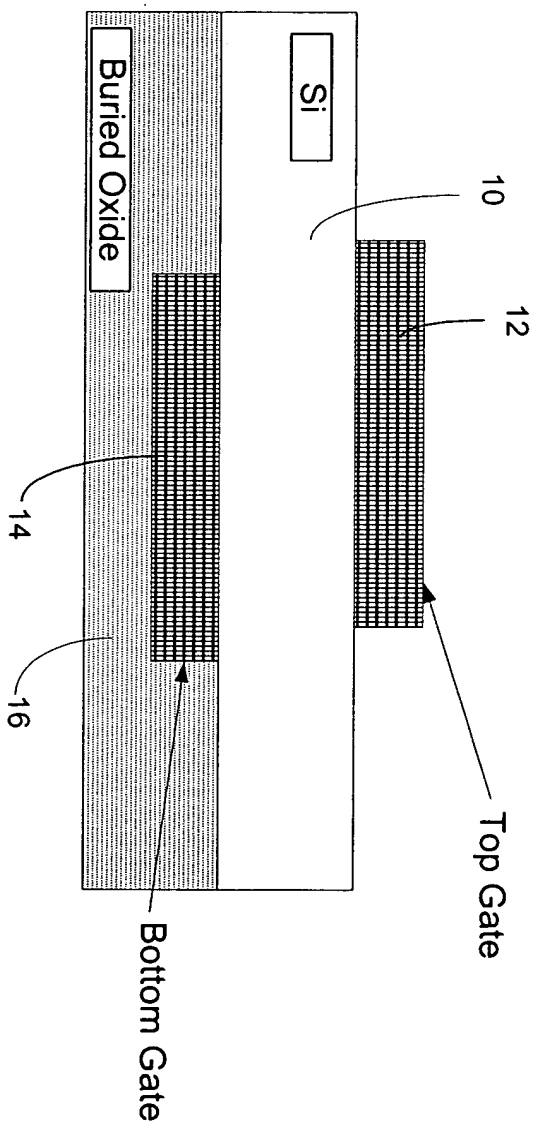
**Docket No.:** AMDI-08399US0

**Attorney:** Stephen R. Bachmann

**Filing Date:** November 13, 2000

**Art Unit:** 2811

**Telephone No.:** 415-362-3800



**FIG. 1**



FIG. 2A

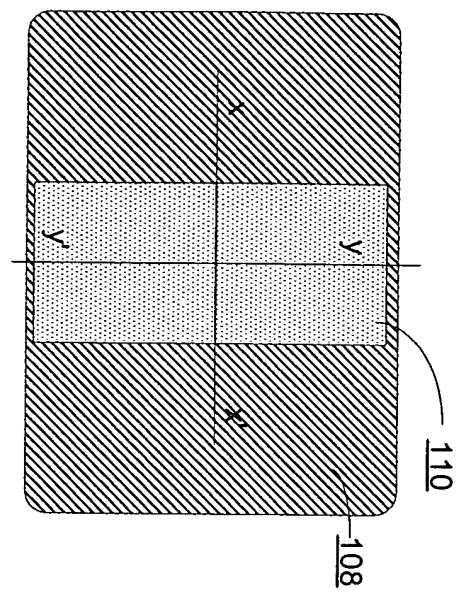


FIG. 2B

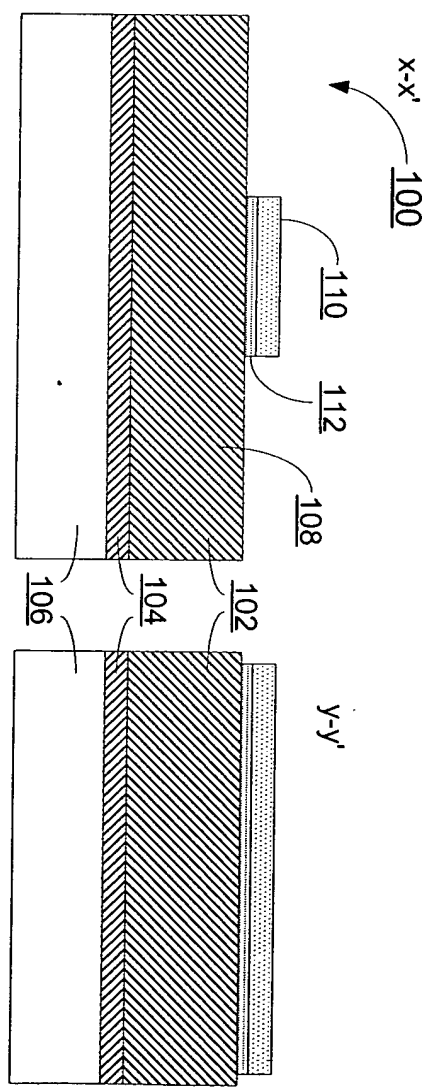


FIG. 2C

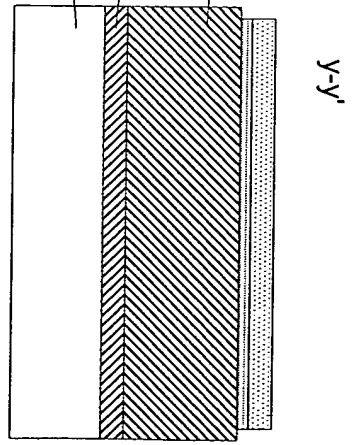


FIG. 3A

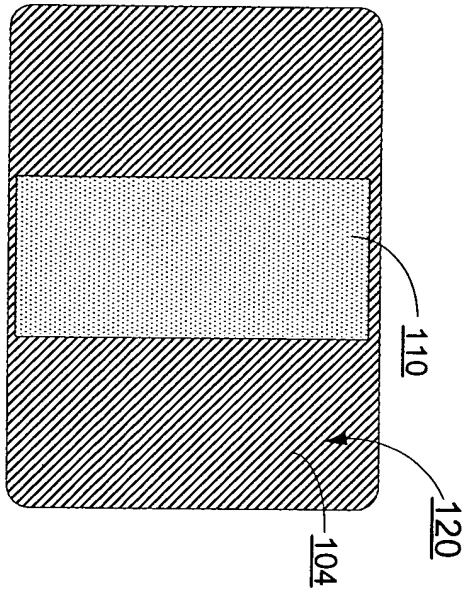


FIG. 3B

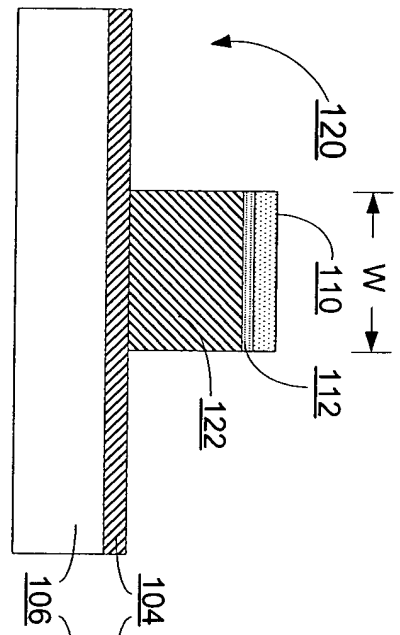


FIG. 3C

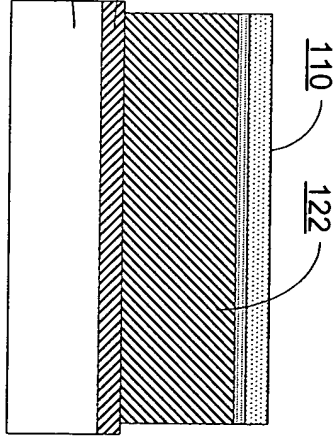




FIG. 4A

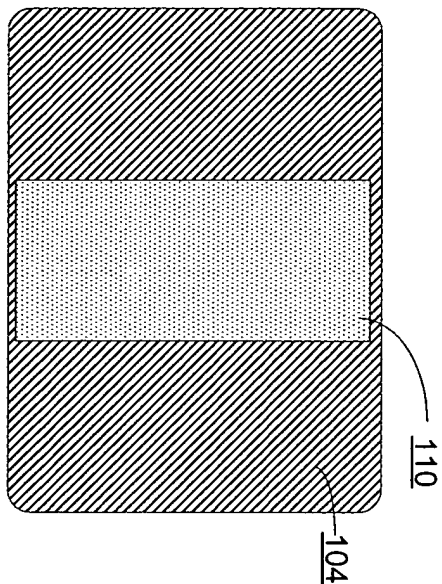


FIG. 4B

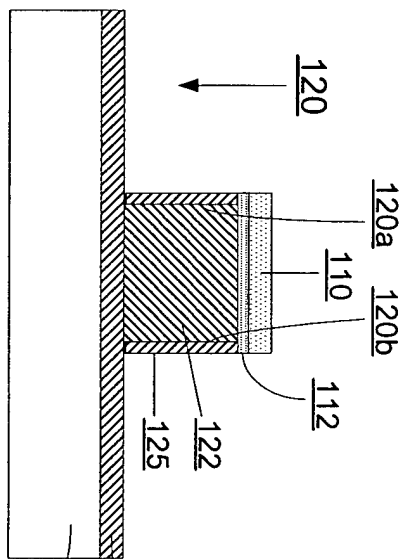
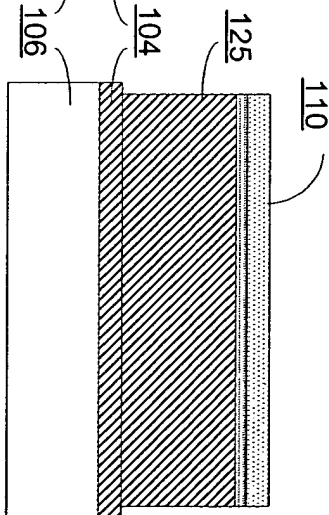


FIG. 4C



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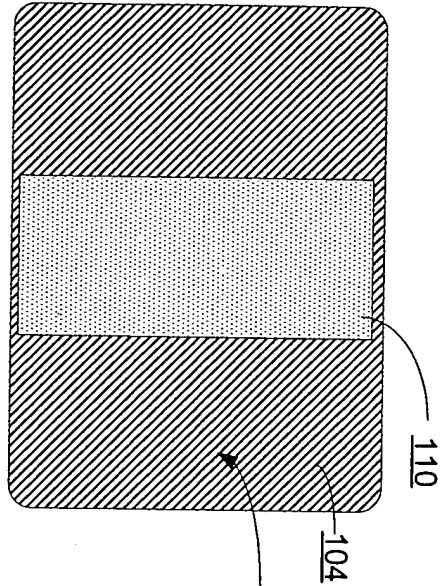


FIG. 5A

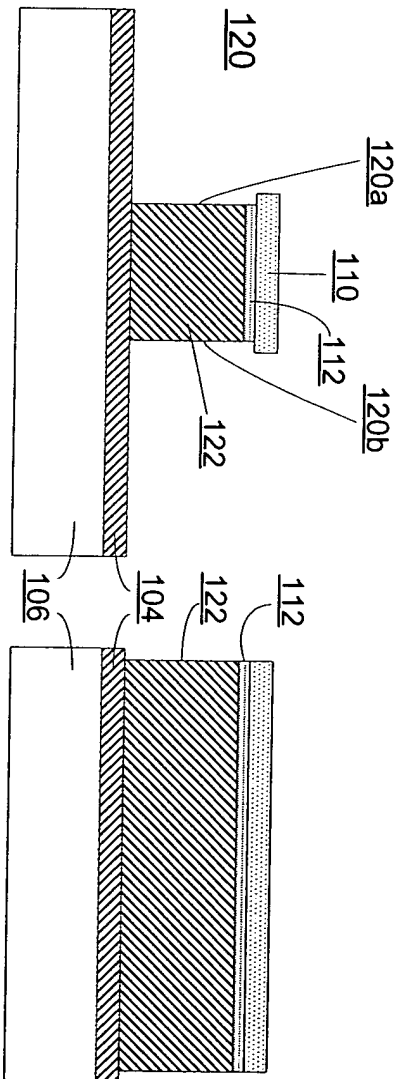


FIG. 5B

FIG. 5C

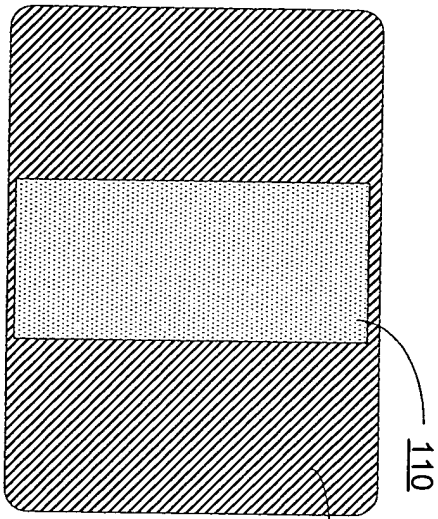


FIG. 6A

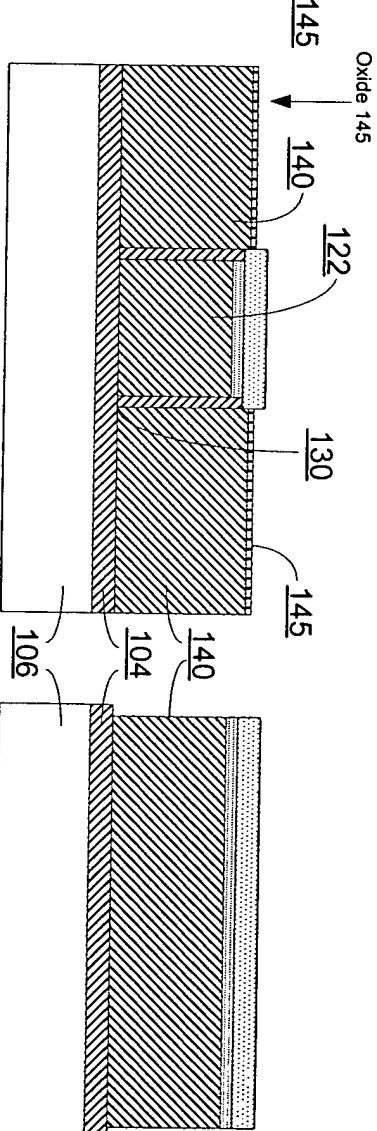


FIG. 6B

FIG. 6C



Title: SELF-ALIGNED TRIPLE GATE SILICON-ON-INSULATOR DEVICE

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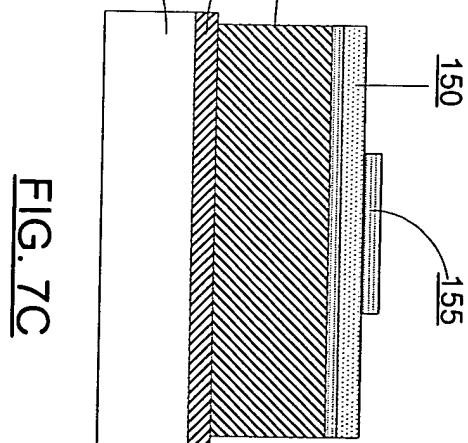
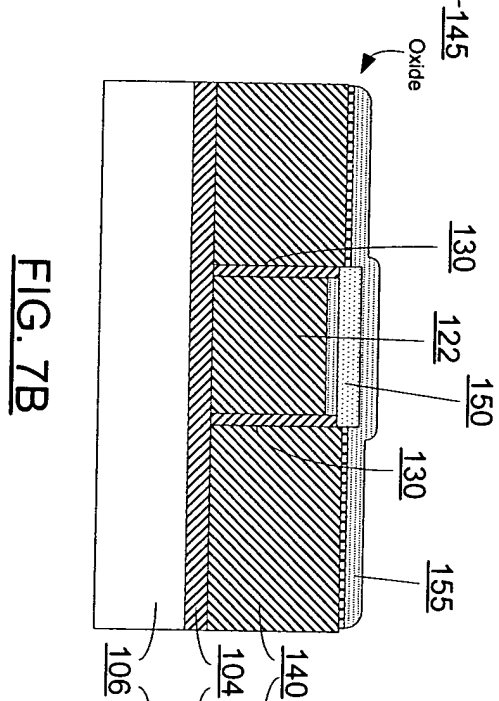
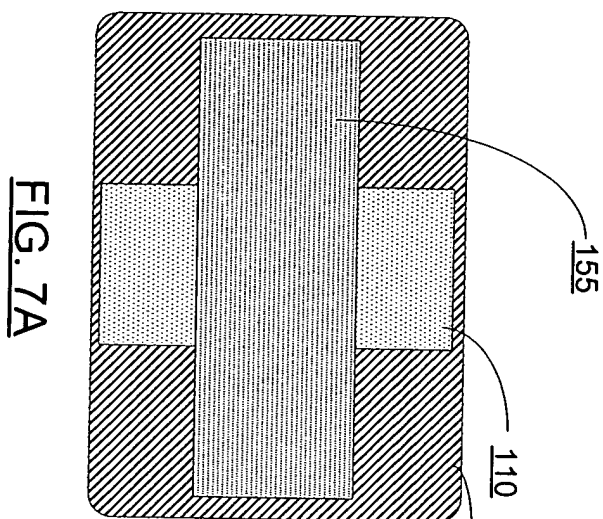
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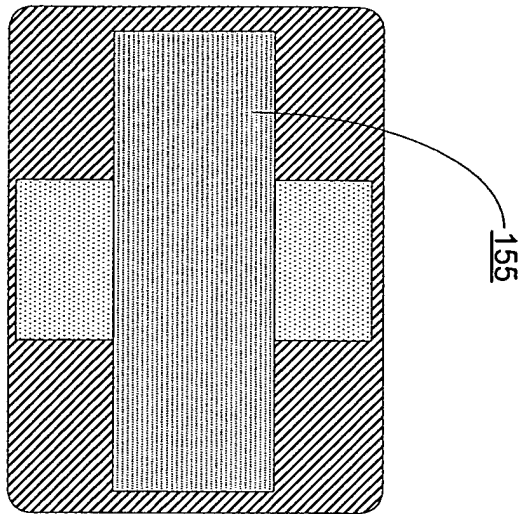


FIG. 8A

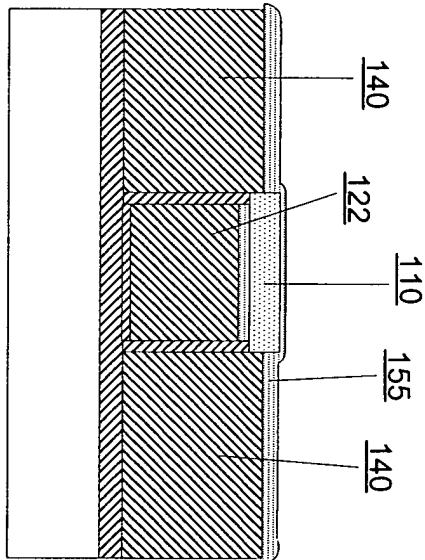


FIG. 8B

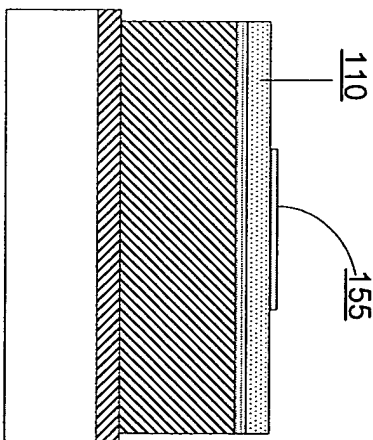


FIG. 8C

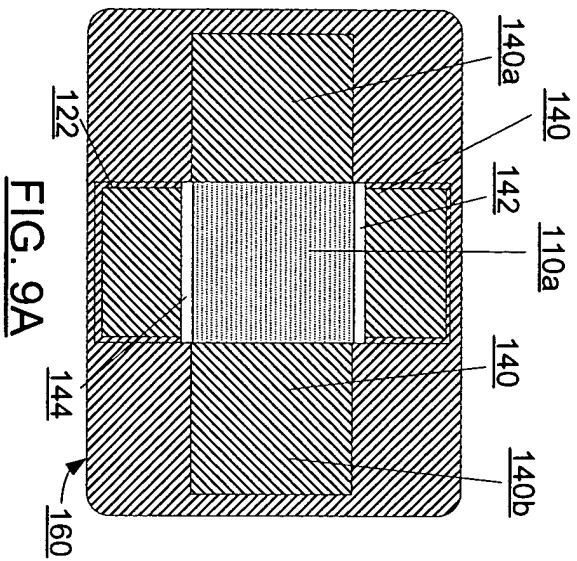


FIG. 9A

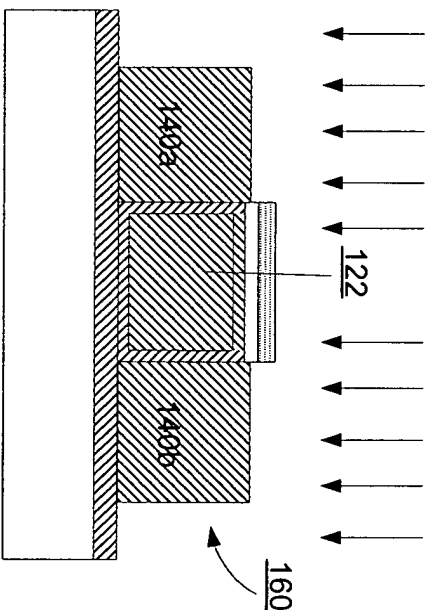


FIG. 9B

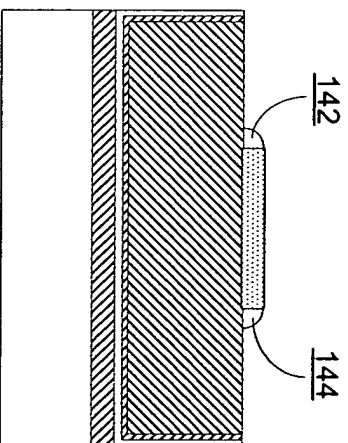


FIG. 9C

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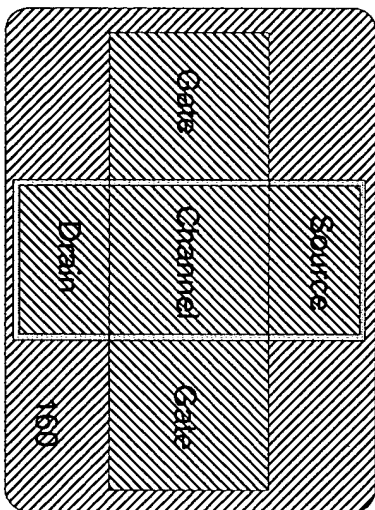


FIG. 10A

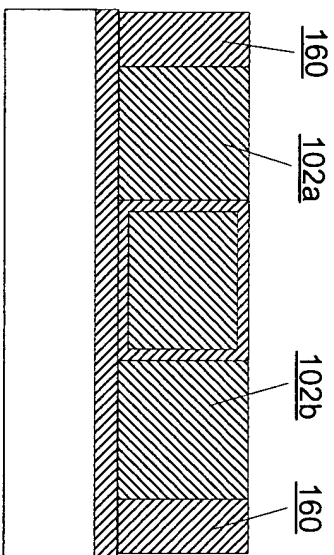


FIG. 10B

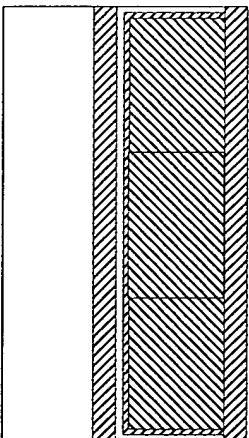


FIG. 10C

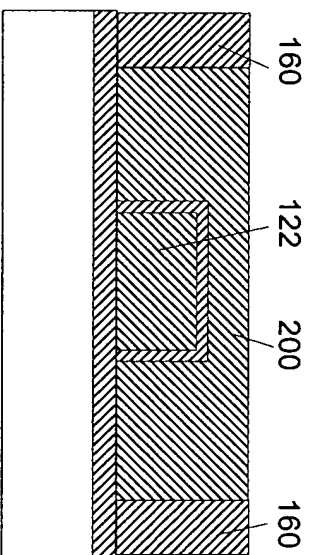


FIG. 11





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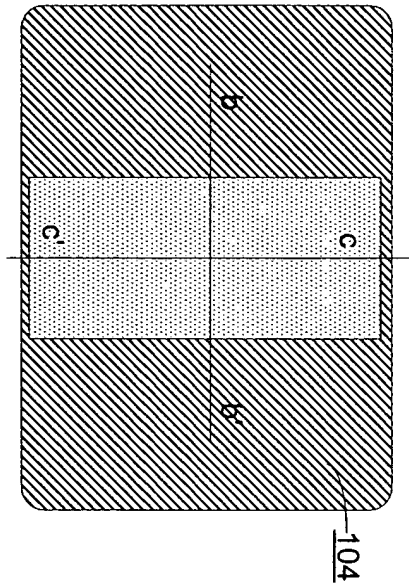


FIG. 12A

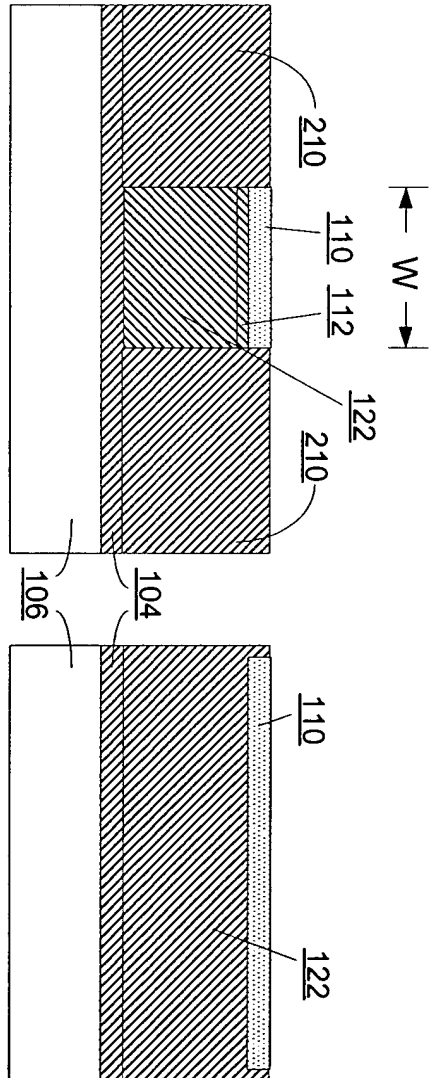


FIG. 12B

FIG. 12C

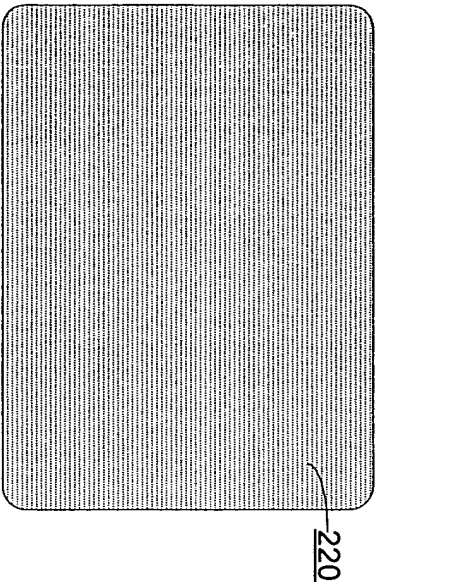


FIG. 13A

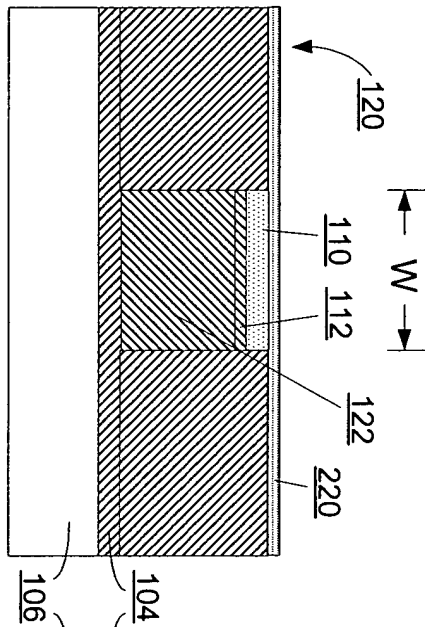
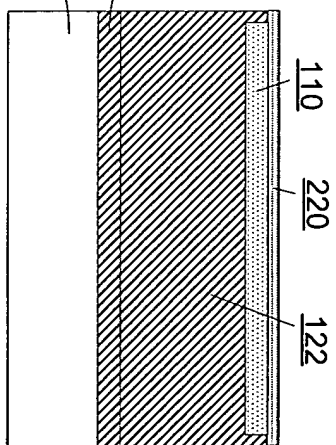


FIG. 13B

FIG. 13C







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FIG. 14A

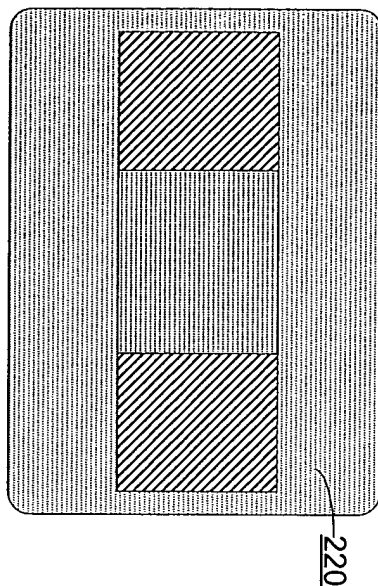


FIG. 14B

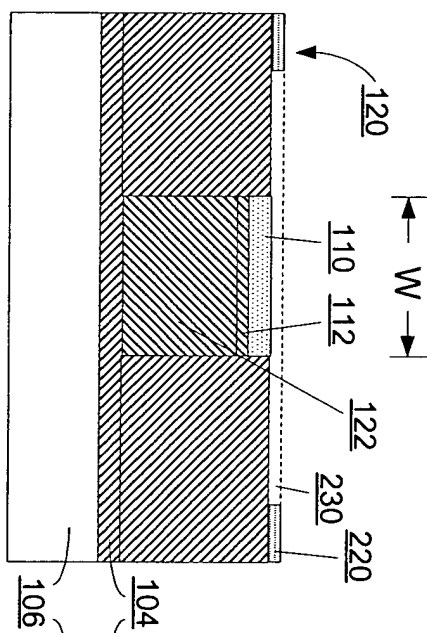
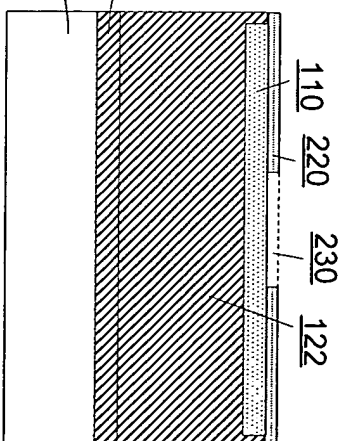


FIG. 14C



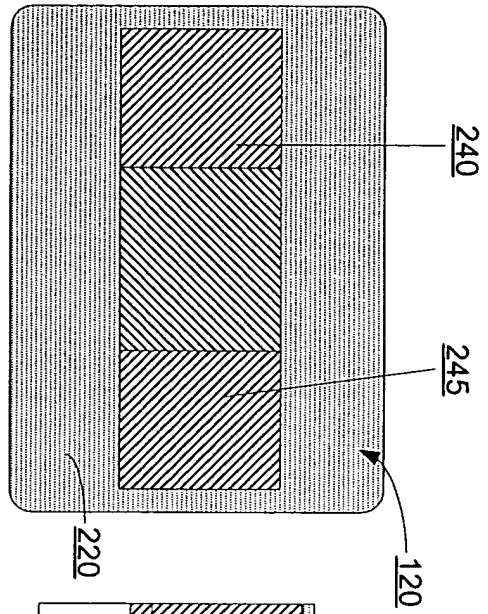


FIG. 15A

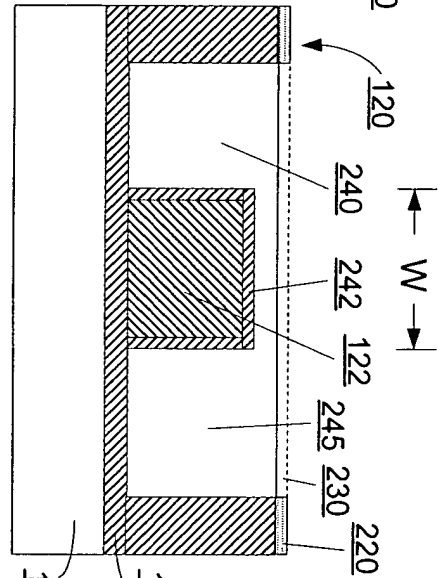


FIG. 15B

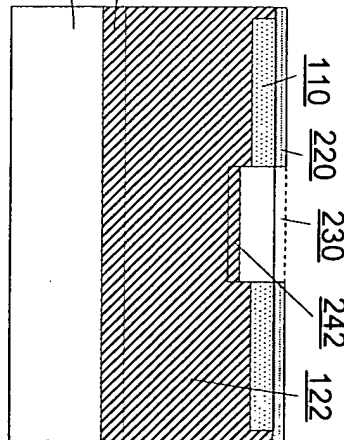


FIG. 15C

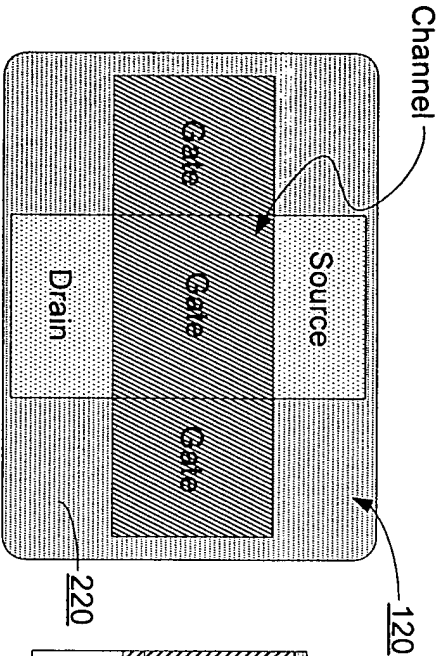


FIG. 16A

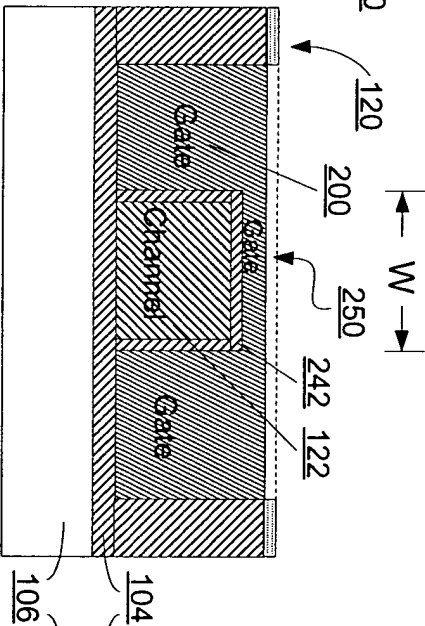


FIG. 16B

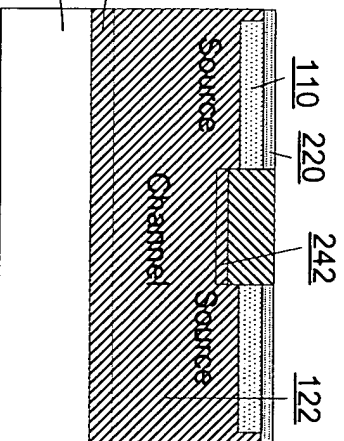


FIG. 16C